On-chip Out-of-Plane High-Q Inductors

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Abstract – Integrating high-Q inductors on semiconductor circuits has been an elusive goal for years due primarily to the eddy current losses and skin effect resistance associated with in-plane spiral inductors. Three-dimensional out-of-plane coils reduce eddy current and skin effect losses by virtue of their geometry and magnetic field orientation. However, out-of-plane coils were not deemed producible by standard semiconductor fabrication methods.

This paper reports on a novel use of conventional semiconductor processing techniques to batch-fabricate three-dimensional high-Q inductors on a wide range of insulating or active semiconductor substrates. Thin molybdenum-chromium films are sputter deposited with an engineered built-in stress gradient so that, when patterned and released from their substrate, they curl into circular springs. These springs self-assemble into three-dimensional scaffolds that form highly conductive windings after being copper plated. Quality factors up to 85 are observed at 1GHz on standard CMOS silicon.

The in-circuit microcoil performance is also compared in BiCMOS silicon L-C oscillators to that of state-of-the-art planar spirals with slotted grounds. A 12.3dB phase-noise improvement is observed with an earlier coil design that produced a maximum Q of 40, and 14.6dB taking the frequency and power differences into account. A 5μm copper layer underneath the coil boosts the quality factor to 85 and should therefore further improve the phase noise by up to 6dB.

I. INTRODUCTION

Transistors, capacitors and resistors are routinely integrated in massive quantities on various semiconductor circuits. The high-quality inductor hasn't been added this list. This hasn't slowed down the development of high-performance digital and baseband analog circuits. But it is increasingly troublesome for the RF front ends in cell phone handsets and mobile data devices. These are rapidly becoming commodity items and economic, thus preferably fully integrated standard CMOS front ends are needed to make next generation wireless devices possible. The quality factor of the current integrated inductors rarely exceeds 8, especially on standard low-resistance CMOS silicon, but values above 50 are often required.

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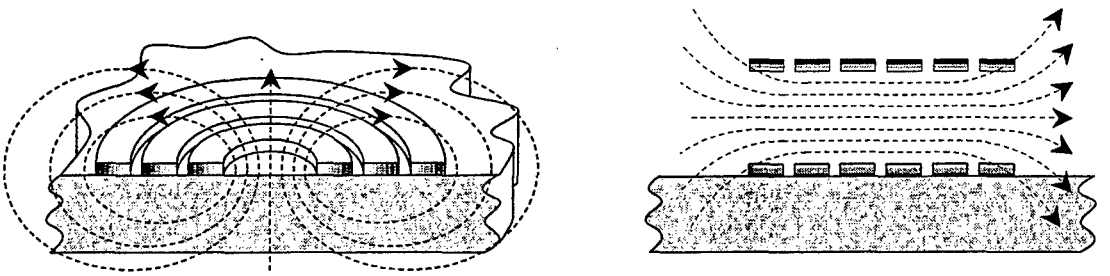

Figure 1. The magnetic flux and current density in conventional planar inductors (left) and out-of-plane solenoids (right). The shading indicates the current density.

Conventional integrated inductors are planar spirals implemented in one or several IC metal layers. These spirals suffer from two fundamental problems (Figure 1, left). First, the magnetic fields are projected straight into the substrate where they induce eddy currents that cause resistive losses. Second, skin and proximity effects push the coil current to the outer winding edge, which reduces the effective winding cross section. As the skin depth for copper at 1GHz is only 2μm, widening the traces does not improve their resistance.

Various configurations have been suggested to deal with these issues. Removing the substrate underneath the coil avoids the eddy currents [1], but leaves the skin effect problem. It is also expensive in terms of wafer real estate, as one cannot put circuits underneath the inductor anymore. Inductors tend to be large compared to the other components because a quality factor fundamentally scales with the inductor size. Lifting spiral inductors out of the wafer plane after processing improves their performance and leaves the substrate available for circuits. Magnetic forces [2] and the surface tension of a molten dot of solder [3] or polymer [4] have been proposed to lift planar structures. However, none of these techniques solve the skin effect problem. This issue has been addressed in the past with very tall windings fabricated by plating copper in a high-aspect ratio mold created in UV-sensitive SU-8 photoresist [5] or by LIGA[2] processing [6], [7]. Unfortunately, producing tall structures is difficult and often expensive, and the substrate eddy current losses remain unaddressed.

Out-of-plane inductors with a coil axis parallel to the substrate plane offer an answer to both issues (Figure 1, right). The bulk of the magnetic flux runs above the circuit substrate. Skin and proximity effects push the coil current to the outer winding surface rather than its edge. Widening the traces, a straightforward lithographical step, now does reduce the winding resistance. Out-of-plane solenoids were initially made by plating a connection between traces above and below a thick dielectric [8] but they were not tall enough for optimal Q. The bond wire microcoils in [9] have the appropriate large cross section, but the bond wire is too thin for optimal Q. Yoon *et al* present an out-of-plane solenoid with large cross section and ribbon windings [10], [11] using three-dimensional laser lithography on coil cores individually picked and placed on the wafer surface. The geometry approaches the ideal cylindrical solenoid of Figure 1, but the process seems difficult to scale to large volume production.

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[2] LIGA is a German acronym for Lithographie, Galvanoformung, Abformung (lithography, galvanoforming, molding).

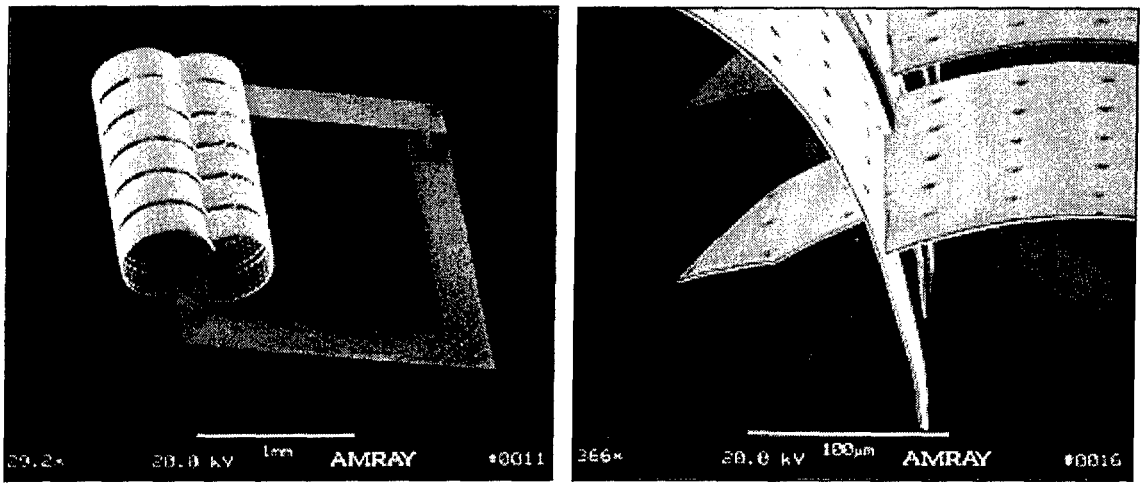

Figure 2. Self-assembled scaffold of a 6-turn out-of-plane coil (left) and close up of the interlocking springs (right).

This paper proposes a low-temperature batch process to micromachine cantilevers with engineered internal stresses that release from the wafer surface and interlock to a scaffold that is then electroplated with low-resistance metal for the coil windings (Figure 2). The solenoid shape is very close to the ideal cylinder and therefore promises excellent RF performance.

II. StressedMetal™ Out-of-plane Microcoils

The cantilevers in Figure 2 are made from a sputtered stress-engineered molybdenum-chromium (MoCr) alloy. MoCr is chosen because it is a refractory metal and can support large internal stresses. It can also be readily wet etched selectively from a host of commonly used release materials.

Stress engineering is accomplished by controlling the ambient pressure during film deposition. Many refractory metals have a common property of acquiring tensile stress when sputtered at high pressures and compressive stress when sputtered at low pressures. At low ambient pressures, sputtered atoms encounter few collisions before reaching the substrate. These energetic atoms tend to pack tighter than their natural arrangement. The tighter atomic arrangement forms compressively stressed films that prefer to expand when "released". Conversely, at high pressures, sputtered atoms loose most of their energy through collisions with ambient atoms before reaching the substrate surface. The sputtered atoms do not have sufficient energy to orient fully to their preferred natural arrangement. Consequently, they tend to form arrangements that are more loosely packed than normal. The film becomes tensile and would contract when released. Figure 3 plots the measured intrinsic stress versus the sputter ambient pressure of MoCr. There is a pressure, about 2.35mTorr in this case, where a stress-free film can be obtained. The exact stress-versus-pressure behavior depends on the sputter conditions, the substrate, and other process parameters and must be characterized for each particular configuration.

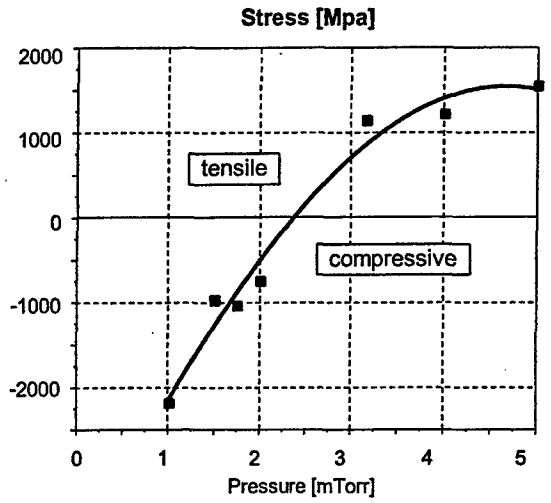

Figure 3. Stress versus sputter ambient pressure of MoCr alloy.

A film that is compressive at the bottom and tensile on the surface will, when patterned and released, curl up with a radius of curvature given by

$$r = h\frac{Y}{\Delta\sigma} \tag{1}$$

where h is the film thickness, Y the biaxial Young's modulus, and $\Delta\sigma$ the stress difference between the surface and bottom of the film [12].

The out-of-plane inductors are assembled from springs in opposite directions so that when released and self-assembled, they curl and interlock in pairs to form the coil windings (a movie of this process is available at http://www.parc.com/solutions/oopcoil/). The self-assembly of this symmetric double-spring structure is more tolerant to radius variations than a simple spring that curls all the way back to the substrate. The 3μm perforations shown on the right of Figure 2 provide extra access points for the etchant to speed up the release.

Unfortunately, good spring materials like MoCr are poor electrical conductors. The assembled spring structure is therefore electroplated with a 5 to 10μm thick copper skin. This also electroforms the interlocked spring tips to a permanent, continuous and solid structure that safely survives a drop from 1m on a hard tile floor.

With mobile communication applications in mind, a demonstrator coil was designed to operate around 1 GHz with a few nH inductance, a minimal Q of 60 and a parasitic resonance well above 1GHz. The quality factor requirements set the coil size: 200μm springs at a 230μm pitch, and a 267μm spring radius. Ten to 15μm of benzocyclobutene (BCB), a low-loss photo-definable dielectric, separates the microcoil from the substrate and controls the parasitic resonances. Vias through the BCB connect the coil terminals to the underlying circuitry.

Note that the microcoil size can be readily reduced to boost the operation frequency. The minimal coil dimensions are actually limited by the lithography and plating. Three-micron spring structures on a 6um pitch were demonstrated before for high-density interconnects [13]. Preliminary calculations suggest that a 10GHz operation frequency is quite feasible.

Figure 4. Alternative probe configuration: vias connect the probe ground to a metal layer underneath the coil.

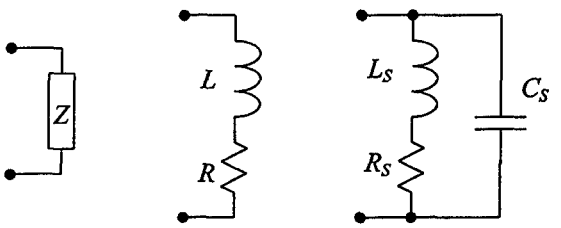

Figure 5. Equivalent L-R and L_S-R_S-C_S coil models.

III. Microcoil Measurements

In order to characterize the microcoil performance, their impedance is measured with an HP4396B combination analyzer and a HP43961A impedance RF test adapter. Each microcoil sample includes a set of ground-signal-ground landing pads for a Cascade Microtech ACP40 GSG-100 probe. The nearest coil terminal connects to the signal pad. The farthest terminal goes to the ground pads either via a loop around the coil (Figure 2) or via a metal layer underneath the coil (Figure 4). The latter configuration minimizes the in-plane inductance and associated losses.

Capacitive parasitics turn the coil impedance real at a resonance frequency ω_0. An analyzer measures the real and imaginary impedance terms R and $X = \omega L$ and thus lumps the resonance effects in the parameters L and R (Figure 5). A series L_S-C_S-R_S model separates the resonance from the inductance and loss resistance, and therefore allows a better understanding of the loss physics. Also, in a circuit where the coil is connected to a loss free capacitor, Q_S $(= \omega L_S/R_S)$ and not Q $(= \omega L/R)$ expresses the tank quality factor. The following expressions allow converting L-R data to L_S-C_S-R_S data [9]. Expression (2) for Q_S is exact. The L_S and R_S expressions are approximations for $|(\omega_0/\omega)^2 - 1| >> 1/Q_S$ but are numerically more stable near coil resonance than their exact versions.

$$Q_S = \left[Q \pm \sqrt{Q^2 + 4\left(\frac{\omega}{\omega_0}\right)^2\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)} \right] \left[2\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right) \right]^{-1} \quad \begin{cases} + \text{ for } \omega < \omega_0 \\ - \text{ for } \omega > \omega_0 \end{cases} \tag{2}$$

$$R_S \approx R\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right)^2, \quad L_S \approx L\left(1-\left(\frac{\omega}{\omega_0}\right)^2\right) \text{ and } C_S = \frac{1}{\omega_0^2 L_S} \tag{3}$$

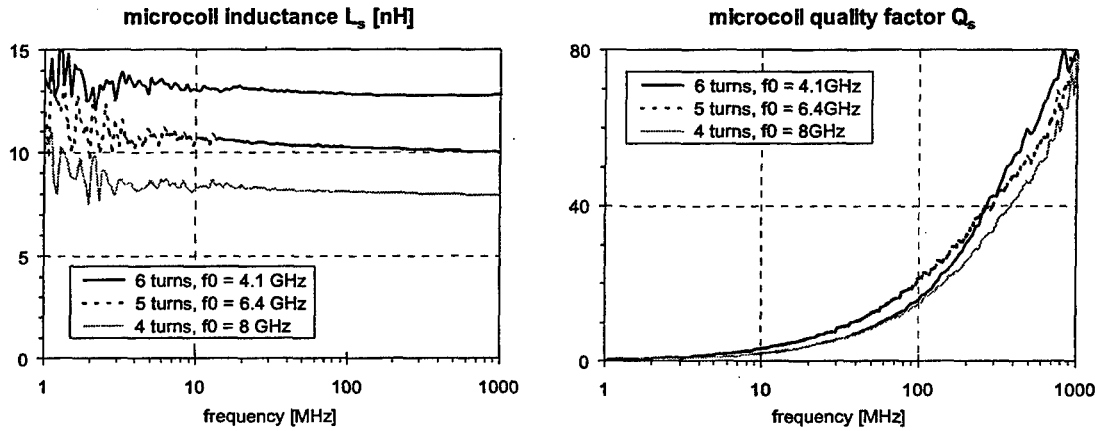

Figure 6. Inductances L_s (left) and Q_s factors (right) of out-of-plane coils on glass and quartz substrates. (f_0 is the parasitic resonance frequency). The probe pads are configured as shown on Figure 2.

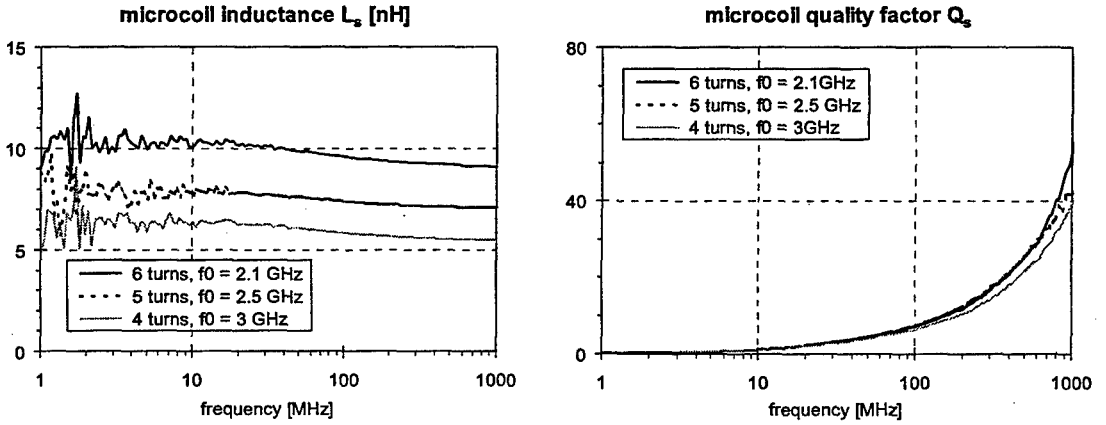

Figure 7. Inductances L_s (left) and Q_s factors (right) of out-of-plane coils on 15 to 20Ω.cm silicon (f_0 is the parasitic resonance frequency). Note the somewhat lower inductance compared to Figure 5 because of the alternative probe configuration.

Figure 6 plots L_S and Q_S data for a number of microcoils on glass and quartz. These data are an excellent a benchmark to compare the values on silicon against. The initial samples on silicon (Figure 7) had a probe configuration as shown in Figure 4 with the return current flowing in a 1μm aluminum on 50nm titanium-tungsten layer, comparable to the top metal on a conventional silicon circuit wafer. Although their quality factors rival the best values found in literature, they do show some substrate loss. Field simulations indicated eddy currents in the substrate and the aluminum near the solenoid ends. Lab experiments also confirmed that the 53mΩ/square aluminum was too resistive. A 5μm thick 5mΩ/square copper layer was therefore adopted to allow the eddy currents to run freely so they shield the silicon from the magnetic fields, but without causing significant resistive loss (Figure 8). The resulting quality factors of 60 to 85 at 1GHz represent an 8 to 10x improvement in comparison to the best spiral inductors on unaltered CMOS silicon that we are aware of.

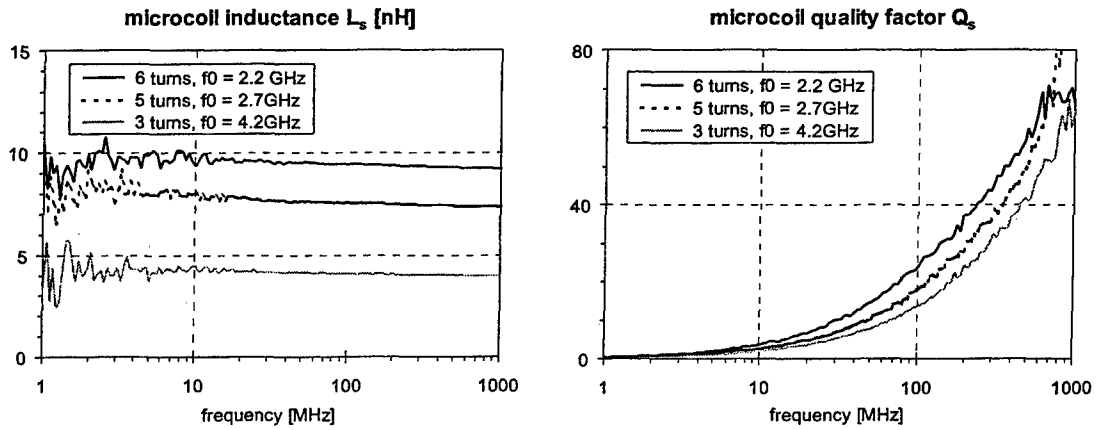

Figure 8. Inductances L_s (left) and Q_s factors (right) of out-of-plane coils on 15 to 20Ω.cm silicon with a 5μm copper layer for the return current (f_0 is the parasitic resonance frequency).

IV. OSCILLATOR

Leeson describes how the close-in phase noise of an oscillator relates to the quality factor of its loaded resonator [15]-[17]. The higher the quality factor, the lower the close-in phase noise. Oscillators are therefore often used to characterize in-circuit inductor performance.

The StressedMetal coils were compared in single ended and balanced L-C oscillators against state-of-the-art integrated spiral inductors with slotted ground planes [18]. The four oscillators were implemented on a chip (Figure 9) in a commercial 0.6μm BiCMOS silicon process (X-FAB XB06, 2 metals, 15GHz f_{Tmax} for the RF NPN BJT). The out-of-plane coils were configured as in our first design with the return currents flowing in the IC top metals. The oscillators shared a common architecture but the component values were optimized to each specific inductor. They were designed to operate around 1GHz but no attempt was made to match the frequencies.

The oscillator phase noise was measured with an HP8561E spectrum analyzer equipped with an HP85671A phase noise utility. As expected, the balanced oscillators outperformed the single ended designs because of the lower supply noise. In the balanced oscillators, a 12.3dB phase-noise improvement was observed with the StressedMetal inductors (TABLE 1), and 14.6dB taking the frequency and power differences into account [19]. This is in line with a Q improvement of a factor of approximately 4. The planar spirals are believed to have a Q of 8 to 10. The first out-of-plane coil design yielded a Q between 35 and 40 (Figure 7). The new design with a 5μm copper layer between the coil and the circuit substrate double that number (Figure 8) and should therefore further improve the phase noise up to 6dB. Current RF-IC processes frequently provide thick copper as the top metal.

Encapsulating the out-of-plane inductor in Dexter HISOL FP4511 epoxy did not influence the oscillator phase-noise. The microcoils were also found much sturdier than conventional 25μm bond wires. The StressedMetal coil technology is therefore believed to be compatible with standard injection molding IC packaging.

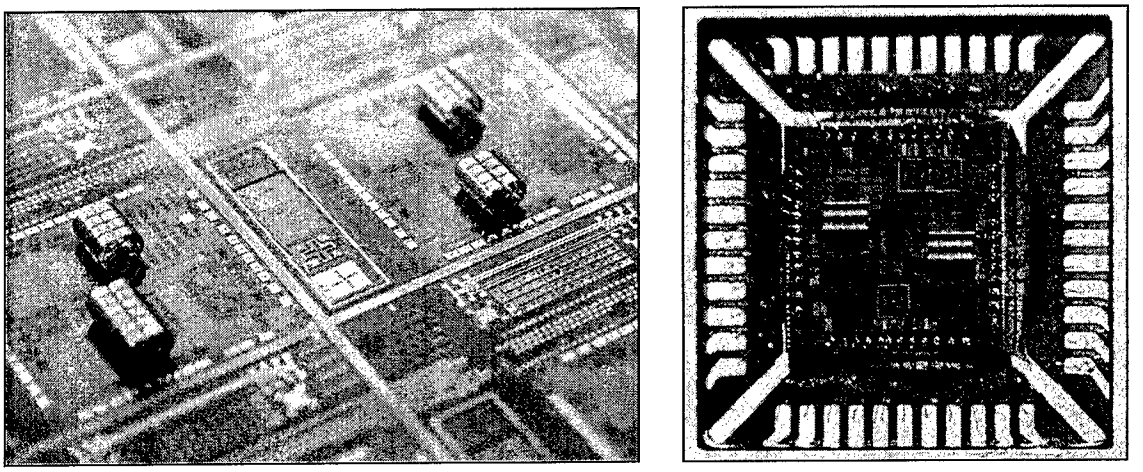

Figure 9. Out-of-plane inductors integrated on a BiCMOS silicon circuit wafer, before (left) and after (right) dicing and packaging. This prototype sports four oscillator cores: a single ended and a balanced circuit with either a conventional planar spiral on a patterned ground or an out-of-plane inductor.

TABLE 1. CIRCUIT RESULTS FOR THE BALANCED OSCILLATORS.

	Planar inductor	Out-of-plane inductor	
f_{osc}	966.6	1215	MHz
V_{CC}	3.3	3.3	V
I_{CC}	20	21	mA (incl. output buffers)
	3..4	3..4	mA (oscillator core only)
P_{out}	-1.2	-1.5	dBm in a 50Ω load
PN	-98.6	-110.9	dBc/Hz @ 100kHz offset

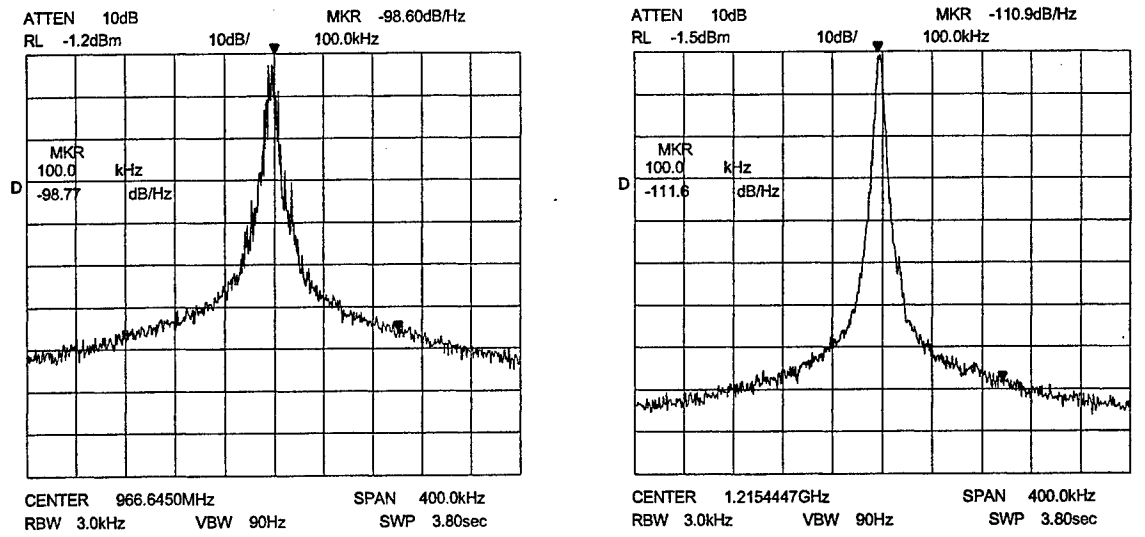

Figure 10. Phase noise plots of the balanced oscillators with planar spiral inductor (left) and with out-of-plane StressedMetal inductor (right).

V. Conclusions

The StressedMetal technology offers a new way to batch-process high-Q out-of-plane inductors by standard semiconductor fabrication methods on wide range of substrates, including active circuit wafers. Three-dimensional out-of-plane coils reduce eddy current and skin effect losses by virtue of their geometry and magnetic field orientation.

The demonstrator coils on 15 to 20Ω.cm silicon showed quality factors up to 85 at 1 GHz. The performance and manufacturability suggest substantial improvement over out-of-plane inductors previously reported.

To explore the circuit performance improvements obtainable with these inductors, coils of both the spiral (with slotted ground plane) and out-of-plane type were fabricated side by side on a chip manufactured in a commercial 2-metal 0.6μm BiCMOS silicon process. Each oscillator was optimized to its specific inductor. A 12.3dB phase-noise improvement was observed with an initial coil design that produced maximum Q's of 40, and 14.6dB taking the frequency and power differences into account. A 5μm copper layer between the coil and the circuit substrate, a feature that is often available with current RF-IC processes, should further improve the noise by up to 6dB.

Because this MEMS structure does not move after self-assembly, inexpensive molded packages with integrated coils should be feasible. Encapsulating the coils with Dexter HISOL FP4511 material did not affect the oscillator phase noise or measured quality factor.

VI. Acknowledgements

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VII. References

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